CLAIM AMENDMENTS

1. (Canceled).

2. (Currently Amended) ~~The~~ A trace circuit ~~according to claim 1,~~ built into a debugging circuit that is, in turn, built into a microcomputer for program debugging, said trace circuit tracing data on a bus of the microcomputer according to a bus clock signal and outputting a result to an emulator, said trace circuit comprising:

a plurality of trace buffer memories in which the data on the bus of the microcomputer is stored according to the bus clock signal;

a control circuit storing the data on the bus in said trace buffer memories, cyclically and in a predetermined order, outputting the data stored in said trace buffer memories, cyclically and in a predetermined order, wherein

the storage of data in and output of data from said trace buffer memories is synchronized with the bus clock signal, and

said control circuit checks the number of bits of the data on said bus, and, if the number of bits of the data on said bus is no larger than a predetermined value, said control circuit stores the data on the bus in only some of said trace buffer memories, and outputs the data stored in said trace buffer memories, cyclically and in predetermined order; and

an output terminal through which the data stored in said trace buffer memories is output to the emulator.

3. (Original) The trace circuit according to claim 2, wherein the predetermined value is 4 bits.

4. (Currently Amended) The trace circuit according to claim ~~1~~ 2 further comprising a bit width conversion circuit connected between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes ~~a~~ bit width of the data to be output from said output terminal based on bit width of the emulator.

5. (Currently Amended) The trace circuit according to claim ~~1~~ 4 further comprising output latch circuits in a number equal to the number of said trace buffer memories and connected between respective trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch outputs of said trace buffer memories.

6. (Canceled).

7. (Currently Amended) ~~The~~ A trace circuit ~~according to claim 6,~~ built into a debugging circuit that is, in turn, built into a microcomputer for program debugging, said trace circuit tracing data on a bus of the microcomputer according to a bus clock signal and outputting a result to an emulator, said trace circuit comprising:

two trace buffer memories in which the data on the bus of the microcomputer is stored according to the bus clock signal;

a control circuit storing the data on the bus in said trace buffer memories cyclically and alternately, outputting the data stored from said trace buffer memories cyclically and alternately, wherein

the storage of data in and output of data from said trace buffer memories is synchronized with the bus clock signal, and

said control circuit checks the number of bits of the data on the bus, and, if the number of bits of the data on the bus is no larger than a predetermined value, said control circuit stores the data on the bus in only ~~some~~ one of said trace buffer memories, and outputs the data stored in said trace buffer memories, cyclically and in a predetermined order; and

an output terminal through which the data stored in said trace buffer memories is output to the emulator.

8. (Original) The trace circuit according to claim 7, wherein the predetermined value is 4 bits.

9. (Currently Amended) The trace circuit according to claim ~~6~~ 7 further comprising a bit width conversion circuit connected between said trace buffer memories and said output terminal, wherein said bit width conversion circuit changes ~~a~~ bit width of the data to be output from said output terminal based on bit width of the emulator.

10. (Currently Amended) The trace circuit according to claim ~~6~~ 9 further comprising two output latch circuits respectively connected between said two trace buffer memories and said bit width conversion circuit, wherein said output latch circuits latch outputs of said trace buffer memories.